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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/510,167	NORDMARK ET AL.	
	Examiner	Art Unit	
	Scott M. Sciacca	2146	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 February 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-9 and 11-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-9 and 11-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This office action is responsive to communications filed on February 19, 2008. Claims 2, 3 and 10 have been cancelled and new claim 19 has been added. Claims 1, 4-9 and 11-19 are pending in the application.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 6-9, 11-12, 15-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sonksen (US 2003/0046429) in view of Kawarai et al. (US 2002/0122424).

Regarding Claim 1, Sonksen teaches a method of pipelined processing of a data packet in a processing means comprising at least two processing stages (*"A method and apparatus for packet processing is disclosed. In one embodiment of the invention the method and apparatus is implemented in plurality of pipeline stages"* – See Abstract), said data packet containing information (*"In most instances, each packet includes a payload portion, containing the data, proceeded by a header portion, containing information about the packet such as the source and destination of the*

packet, quality of service, packet size and other information" – See [0002]; The packet includes a payload (information) portion), said method characterised by

generating an intermediate data packet by adding a dummy header and/or dummy tail to said data packet (*"the invention may comprise a method of adding a tag to a packet comprising identifying a control word to guide processing of a packet and then storing a portion of a packet in a memory"* – See [0015]);

associating information reference to said intermediate data packet (*"each packet is associated with a control word"* – See [0025]; *"The control words are generated from information extracted from the packet handle"* – See [0095]; *"The packet handle comprises information about the packet, such as including but not limited to the packet format, packet length or type of service"* – See [0094]);

storing said information reference in additional register (*"In one embodiment the invention comprises a system for dynamically modifying or supplementing the contents of a packet on a packet by packet basis including a first memory configured to store a control word"* – See [0017]); and

processing said intermediate data packet in a processing stage (*"the invention modifies a packet based on control instructions and includes a pipeline processing stage comprising one or more memory modules configured to store packet data and supplemental data"* – See [0019]).

Sonksen goes on to disclose that various fields in a packet may be modified (*"The one or more data modifiers may perform modifications consisting of modification to a time to live value, a type of service value, a checksum value, or other data fields in*

a packet" – See [0022]). Sonksen shows that values such as a time to live value or checksum value must be updated as a packet is processed in order to account for the modifications to the information in the packet (*"In this embodiment the checksum generator 1340 creates a running total of the value of the bytes in a packet. The use of a checksum for error checking is know in the art and accordingly not described in great detail here. If a packet is modified it may be desired to modify the checksum to account for the modification"* – See [0112]). Thus, Sonksen generally teaches as shown above that certain fields in a packet are modified to account for changes to the information in the packet. Sonksen does not explicitly teach that the information reference comprises information relating to the length and position of the information of the data packet contained in the intermediate data packet. However, Kawarai discloses a packet containing parameters regarding a length and position of the information (payload portion) of a data packet (*"Offset Value indicates the start position of a valid field for payload information in a fixed-length packet. Payload Length indicates the length of the valid field from that start position"* – See [0053]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to associate with a packet the length and position of information within said packet. Motivation for doing so would be to provide information regarding the location of the "useful" data otherwise known as the payload of a packet so that the packet may be handled properly when received (See Kawarai, [0056]).

Regarding Claim 6, Sonksen teaches said information reference being included in additional information associated with said intermediate data packet (*"Note that in different formats or protocols the entire header may be of different length, items of information may be arranged in different order, pieces of information in the header may be of different length, or additional items of information may be included. Advantageously the dynamic processing module of the invention is able to dynamically adapt and/or accommodate the various different header formats and the challenges presented by different formats"* – See [0081]; As shown above with regard to Claim 1, the information reference (position and length of an information item within a packet) is taken into consideration when the corresponding packet is processed).

Regarding Claim 7, Sonksen further teaches that prior to said step of processing said intermediate data packet, said information reference is stored in at least one register accessible to the processing stage performing said processing (*"The method may also include storing associated packets and control words prior to entry of a packet into the processing pipeline"* – See [0033]).

Regarding Claim 8, the combination of Sonksen and Kawarai teaches the information reference comprising a length value and an offset value, said length value representing the length of the information contained in said intermediate data packet and said offset value indicating the position in said intermediate data packet of the information contained in said data packet as shown above with respect to Claim 1.

Regarding Claim 9, Sonksen teaches a processing means for pipelined processing of a data packet (*"FIG. 3 illustrates a block diagram of an example embodiment of a pipeline packet processing system of the invention"* – See [0037]), said processing means comprising at least one processing stage comprising a logic unit (*"Shown in FIG. 3 is a first processing module 312, a second processing module 320 up to an Nth processing module 328"* – See [0062]) and a register for storing at least part of said data packet (*"In one embodiment the input line 300 may carry packets and associated control data to the memory 308 for storage"* – See [0061]), said processing means being characterised in that

a receiver is adapted to receive said data packet and to generate an intermediate data packet by adding a dummy header and/or a dummy tail to said data packet (*"The dynamic processing module 502 comprises a module that may be configured to generate or modify a tag or other portion of a packet header, such as a tag that may be attached to a portion of a packet to aid in packet processing or routing"* – See [0068]);

at least one register for storing information reference associated with said intermediate data packet is accessible to said logic unit (*"In one embodiment the invention comprises a system for dynamically modifying or supplementing the contents of a packet on a packet by packet basis including a first memory configured to store a control word"* – See [0017]; *"According, a first controller 316 connects or communicates with the memory 308 and the first processing module 312"* – See [0062]); and

at least one of at said at least one logic units is adapted to operate upon said information reference (*"The first processing module 312 processes the data in accordance with the controller 316"* – See [0063]).

Sonksen does not explicitly teach the information reference comprising information relating to the length and position of the information of the data packet contained in said intermediate data packet. However, Kawarai discloses a packet containing parameters regarding a length and position of the information (payload portion) of a data packet (*"Offset Value indicates the start position of a valid field for payload information in a fixed-length packet. Payload Length indicates the length of the valid field from that start position"* – See [0053]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to associate with a packet the length and position of information within said packet for the same reasons as those given with respect to Claim 1.

Regarding Claim 11, Sonksen teaches said receiver for adding comprising a buffer (*"FIG. 8 illustrates an example implementation of one example embodiment of the tag generation module"* – See [0043]; *"In the embodiment shown in FIG. 8, the FIFO unit 800 includes control word/label storage 804 and packet data storage 806"* – See [0083]) and a shifter (*"In the example embodiment shown in FIG. 8, the second register 844 includes four byte shift registers"* – [0087]).

Regarding Claim 12, Sonksen teaches the means of Claim 9 further comprising means for removing at least one bit from said intermediate data packet (*"It also includes a processing module configured to add supplemental data to a packet or strip data from a packet based on control instructions and the processing location in the packet"* – See [0019]).

Regarding Claim 15, Sonksen teaches said at least one register for storing information reference being located in said processing stage (Each processing module in Fig. 3 includes an interface to memory 308).

Regarding Claim 16, Sonksen teaches said at least one register for storing information reference comprising one register and another register (*"This system may include a control word bank having two or more locations"* – See [0025]). As shown above with regard to Claim 1, Hultsch teaches that the values may be a length value and an offset value.

Regarding Claim 17, Sonksen teaches an integrated circuit characterized by processing means according to Claim 9 (*"In one embodiment an the method and apparatus is enabled in an ASIC-based solution"* – See [0012]; The processing means is characterized by an ASIC (application-specific integrated circuit)).

Regarding Claim 18, Sonksen teaches a computer unit characterized by an integrated circuit according to Claim 9 (*"In one embodiment an the method and apparatus is enabled in an ASIC-based solution"* – See [0012]; The processing means is characterized by an ASIC (application-specific integrated circuit)).

Regarding Claim 19, Sonksen teaches a pipelined processor for processing a data packet, comprising:

a register for storing at least part of the data packet (*"invention may comprise a method of adding a tag to a packet comprising identifying a control word to guide processing of a packet and then storing a portion of a packet in a memory"* – See [0015]);

at least one additional register for storing an information reference for association with an intermediate data packet (*"In one embodiment the invention comprises a system for dynamically modifying or supplementing the contents of a packet on a packet by packet basis including a first memory configured to store a control word"* – See [0017]);

a logic unit performing-the steps of:

receiving the data packet (*"an input line 300 receives packets and/or control information to be processed by the pipeline operation"* – See [0061]);

generating the intermediate data packet by adding a dummy header and/or dummy tail to the data packet (*"The dynamic processing module 502 comprises a module that may be configured to generate or modify a tag or other portion of a packet*

header, such as a tag that may be attached to a portion of a packet to aid in packet processing or routing" – See [0068]);

associating information reference to the intermediate data packet (*"each packet is associated with a control word"* – See [0025]; *"The control words are generated from information extracted from the packet handle"* – See [0095]; *"The packet handle comprises information about the packet, such as including but not limited to the packet format, packet length or type of service"* – See [0094]);

storing the information reference in the at least one additional register (*"In one embodiment the invention comprises a system for dynamically modifying or supplementing the contents of a packet on a packet by packet basis including a first memory configured to store a control word"* – See [0017]); and

processing the intermediate data packet in a processing stage (*"The first processing module 312 processes the data in accordance with the controller 316"* – See [0063]).

Sonksen goes on to disclose that various fields in a packet may be modified (*"The one or more data modifiers may perform modifications consisting of modification to a time to live value, a type of service value, a checksum value, or other data fields in a packet"* – See [0022]). Sonksen shows that values such as a time to live value or checksum value must be updated as a packet is processed in order to account for the modifications to the information in the packet (*"In this embodiment the checksum generator 1340 creates a running total of the value of the bytes in a packet. The use of a checksum for error checking is know in the art and accordingly not described in great*

detail here. If a packet is modified it may be desired to modify the checksum to account for the modification" – See [0112]). Thus, Sonksen generally teaches as shown above that certain fields in a packet are modified to account for changes to the information in the packet. Sonksen does not explicitly teach that the information reference comprises information relating to the length and position of the information of the data packet contained in the intermediate data packet. However, Kawarai discloses a packet containing parameters regarding a length and position of the information (payload portion) of a data packet (*"Offset Value indicates the start position of a valid field for payload information in a fixed-length packet. Payload Length indicates the length of the valid field from that start position"* – See [0053]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to associate with a packet the length and position of information within said packet for the same reasons as those given with respect to Claim 1.

3. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sonksen (US 2003/0046429) in view of Kawarai et al. (US 2002/0122424) and further in view of Hultsch (WO 99/60708).

Regarding Claim 4, Sonksen further teaches upon said intermediate data packet exiting the last of said at least one processing stages removing from said intermediate data packet (*"The dynamic stages are configured to modify, remove, or supplement portions of the packet as the packet or portion thereof passes through the pipeline with*

the aid of a more flexible control structure. The static stages are configured to modify, remove, or supplement portions of the packet as the packet or portion thereof passes through the pipeline with the aid of a hardwired system" – See Abstract; As shown in Fig. 5A the pipeline includes at least two stages, one dynamic and one static, both of which may remove bits from a packet).

Sonksen and Kawarai do not explicitly teach the removal being based on a determination of whether any bits of said intermediate data packet are superfluous. However, Hultsch discloses removing superfluous data from a packet (*"removing the superfluous filler data received via the circuit-switched connection in the data stream (DS1) with the constant data rate and by reformatting the useful data for the data stream with the variable data rate and sending it via a packet-orientated connection"* – See Abstract). Motivation for doing so would be to make efficient use of transmission bandwidth (See Hultsch, Abstract).

Claim 5 is rejected using the same reasoning as that was given above with regard to Claim 4.

4. Claims 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sonksen (US 2003/0046429) in view of Kawarai et al. (US 2002/0122424) and further in view of Lee et al. (US 6,996,117).

Regarding Claim 13, Sonksen teaches means for removing comprising a buffer (*"FIG. 17 illustrates an example embodiment of a data modifier system as may be contemplated for use with a pipeline processing system"* – See [0054]; *"Register 1704 has sections A, B, C and D"* – See [0125]), but does not explicitly teach means for removing also comprising a shifter. However, Lee does teach using a shifter as means for removing data (*"The stripped-off information element segment 450 is rotated backward by one place (i.e., shifted to the left by one place) to produce the rotated information element segment 452"* – See Col. 29, lines 65-67). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a shifter as means for removing at least one bit of data. Motivation for doing so would be to implement as much of the processing means as possible in hardware in order to boost performance (See Col. 1, lines 65-67 of Lee's disclosure).

5. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sonksen (US 2003/0046429) in view of Kawarai et al. (US 2002/0122424) and further in view of Song (US 5,818,894).

Regarding Claim 14, Sonksen teaches means for adding comprising a shifter (See above remarks regarding Claim 11), but does not explicitly teach the shifter being a barrel shifter. However Song does teach a barrel shifter with inputs for adding input data (*"A high speed barrel shifter in which fill input data is especially added"* – See Abstract; *"FIG. 1 is a block diagram of an 8-bit barrel shifter according to the present*

invention" – See Col. 1, lines 61-62). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a barrel shifter as means for adding at least one bit to a packet of data. Motivation for doing so would be to provide a device which can perform shift operations at high speed while minimizing the necessary logic circuitry (See Col. 1, lines 25-27 of Song's disclosure).

Response to Arguments

6. Applicant's arguments filed on February 19, 2008 have been fully considered but they are not persuasive.

On page 12, lines 15-16 that Sonksen "does not disclose a dummy header or dummy tail in a generated data packet".

Examiner would like to point out that a header or tail in its broadest sense is just data about the packet. Many common examples demonstrate a header being inserted at the beginning of a packet and likewise, a tail being inserted at the end. However, this is not necessary or inherent. Based on Figure 1 and the accompanying description in the present invention, a header could be placed in any sequence relative to the payload data of the packet. As shown above with respect to Claim 1, Sonksen teaches inserting a dummy header into a packet in the form of a tag (*"the invention may comprise a method of adding a tag to a packet comprising identifying a control word to guide processing of a packet and then storing a portion of a packet in a memory"* – See

[0015]). The same reasoning applies to Applicant's arguments regarding Claims 9 and 19.

7. The rest of Applicant's arguments with respect to Claims 1, 9 and 19 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott M. Sciacca whose telephone number is (571) 270-

1919. The examiner can normally be reached on Monday thru Friday, 7:30 A.M. - 5:00 P.M. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeff Pwu can be reached on (571) 272-6798. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/S. M. S./
Examiner, Art Unit 2146

/Jeffrey Pwu/
Supervisory Patent Examiner, Art Unit 2146